VELTECH MULTI TECH

Dr RANGARAJAN Dr. SAKUNTHALA ENGINEERING COLLEGE

(Owned by Vel Trust 1997)

(An ISO 9001: 2008 Certified Institution)

Accredited By NAAC with 'A' Grade and NBA Accredited Institution

(Approved by AICTE New Delhi and Govt. of Tamil Nadu, Affiliated to Anna University Chennai)

SYLLABUS

WEEKLY SCHEDULE

M E VLSI

III SEMESTER 2017 - 2018

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
II YEAR DEGREE COURSE

#42, Avadi – Vel Tech Road,
Avadi
Chennai – 600062
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Vision of the Institute

Elevating Well Being of Humanity by Augmenting Human Resource Potential Through Quality Technical Education and Training

Mission of the Institute

To effectuate supremacy in technical education through articulation of research and industry practices for social relevance. To inculcate the habit of lifelong learning To exhibit professional ethics, commitment and leadership qualities

Vision of the Department

To emerge as a centre of academic eminence in electronics and communication and related spheres through knowledge acquisition and propagation meeting global needs and standards

Mission of the Department

- To impart quality education by inculcating fundamental knowledge in electronics and communication engineering with due focus on research and industry practices.
- To propagate lifelong learning.
- To impart the right proportion of knowledge, attitudes and ethics in students to enable them take up positions of responsibility in the society and make significant contributions.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

- PEO1: To prepare students with strong foundation in basic science and mathematics and ability to use these tools in professional career and/or higher education by acquiring knowledge in area of Electronics and Communication Engineering.
- PEO2: Analyze real life problems, design appropriate system to provide solutions that are technically sound, economically feasible and socially acceptable.
- PEO3: To train students with electrical and computer engineering breadth so as to Work on multi-disciplinary projects.
- PEO4: Exhibit professionalism, ethical attitude, communication skills, team work in their profession and adapt to current trends by engaging in lifelong learning.

PROGRAM OUTCOME (POs)

- PO1: Apply knowledge of computing, mathematics, science and engineering fundamentals appropriate to the discipline.
- PO2: Identify, formulate, research literature and solve complex Electronics and Communication Engineering problems for reaching substantial conclusions.
- PO3: Design, implement and evaluate an electronics-based system, process, component or program to the standards for the benefits of the society.
- PO4: Perform investigations of complex problems including design of experiments, analysis and interpretation of data and synthesis of information to provide valid conclusions.
- PO5: Use current techniques, skills and modern engineering tools necessary for computing practice.
- PO6: Demonstrate understanding of the societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to engineering practice.
- PO7: Understand that the solutions have to be provided taking the environmental issues and sustainability into consideration.
- PO8: Understand and commit to professional ethics, responsibilities and norms of engineering practice.
- PO9: Function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings
- PO10: Communicate effectively on complex Electronics and Communication engineering activities with the engineering community and with society at large, such as being able to comprehend, write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- PO11: An understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects.
- PO12: Realize the need for lifelong learning and engage them to adopt technological changes.

WEEK DETAILS

SL.NO.	WEEK	FROM	TO
1	**WEEK1**	**24.06.2017**	**24.06.2017**
2	**WEEK2**	**27.06.2017**	**01.07.2017**
3	**WEEK3**	**03.07.2017**	**08.07.2017**
4	**WEEK4**	**10.07.2017**	**15.07.2017**
5	**WEEK5**	**17.07.2017**	**22.07.2017**
6	**WEEK6**	**24.07.2017**	**29.07.2017**
7	**WEEK7**	**31.07.2017**	**05.08.2017**
8	**WEEK8**	**07.08.2017**	**12.08.2017**
9	**WEEK9**	**16.08.2017**	**19.08.2017**
10	**WEEK10**	**21.08.2017**	**26.08.2017**
11	**WEEK11**	**28.08.2017**	**01.09.2017**
12	**WEEK12**	**04.09.2017**	**09.09.2017**
13	**WEEK13**	**11.09.2017**	**16.09.2017**
14	**WEEK14**	**18.09.2017**	**23.09.2017**
15	**WEEK15**	**25.09.2017**	**28.09.2017**
16	**WEEK16**	**03.10.2017**	**07.10.2017**
17	**WEEK17**	**09.10.2017**	**14.10.2017**

SUBJECT CONTENTS

SL.NO	SUBJECT CODE	SUBJECT NAME
THEORY		
1	VL7301	TESTING OF VLSI CIRCUITS
2	AP 7301	ELECTROMAGNET IC INTERFERENCE AND
3	AP 7010	DATA CONVERTERS
PRACTICAL		
4	VL7311	PROJECT WORK (PHASE I)

TEST / EXAM SCHEDULE

SL.NO	SUBJECT CODE	SUBJECT NAME	UNIT TEST I	UNIT TEST II	Pre Model Exam	UNIT TEST IV
1	VL7301	Testing of VLSI Circuits	10-07-2017 AN	27-07-2017 AN	16.08.2017 AN	07.09.2017 AN
2	AP7301	Electromagnetic Interference and Compatibility	11-07-2017 AN	28-07-2017 AN	17.08.2017 AN	08.09.2017 AN
3	AP7010	Data Converters	12-07-2017 AN	29-07-2017 AN	18.08.2017 AN	09.09.2017 AN

SL.NO	SUBJECT CODE	SUBJECT NAME	MODEL EXAM
1	VL7301	Testing of VLSI Circuits	28.09.2017 AN
2	AP7301	Electromagnetic Interference and Compatibility	04.10.2017 AN
3	AP7010	Data Converters	06.10.2017 AN

VL7301 TESTING OF VLSI CIRCUITS

WEEK 1

UNIT I TESTING AND FAULT MODELLING

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models

WEEK 2

Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation

WEEK 3

Delay models – Gate Level Event – driven simulation.

WEEK 4 UNIT TEST -I

UNIT II TEST GENERATION

Test generation for combinational logic circuits – Testable combinational logic circuit design

WEEK 5

Test generation for sequential circuits

WEEK 6

design of testable sequential circuits.

UNIT TEST -II

WEEK 7

UNIT III DESIGN FOR TESTABILITY

Design for Testability – Ad-hoc design

WEEK 8

generic scan based design – classical scan based design – system level DFT approaches

WEEK 9 &10 – PREMODEL EXAM

UNIT IV SELF – TEST AND TEST ALGORITHMS

Built-In self Test – test pattern generation for BIST

WEEK 11 Circular BIST – BIST Architectures – Testable Memory Design

WEEK 12

Test Algorithms – Test generation for Embedded RAMs.

UNIT TEST -IV

WEEK 13

UNIT V - FAULT DIAGNOSIS

Logical Level Diagnosis – Diagnosis by UUT reduction

WEEK 14

Fault Diagnosis for Combinational Circuits – Self-checking design System Level Diagnosis.

WEEK- 15 MODEL EXAM

WEEK- 16 MODEL EXAM

WEEK- 17 MODEL EXAM

TOTAL: 45 PERIODS

REFERENCES:

1. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable
Design", Jaico Publishing House,2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory
and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

AP7301 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

WEEK 1

UNIT I EMI/EMC CONCEPTS

EMI-EMC definitions and Units of parameters; Sources and victim of EMI

WEEK 2

Conducted and Radiated EMI Emission and Susceptibility

WEEK 3

Transient EMI, ESD; Radiation Hazards

WEEK 4 UNIT TEST -I

UNIT II EMI COUPLING PRINCIPLES

Conducted, radiated and transient coupling; Common ground impedance coupling

WEEK 5

Common mode and ground loop coupling ; Differential mode coupling; Near field cable to cable coupling, cross talk

WEEK 6

Field to cable coupling ; Power mains and Power supply coupling.

UNIT TEST -II

WEEK 7

UNIT III EMI CONTROL TECHNIQUES

Shielding- Shielding Material-Shielding integrity at discontinuties, Filtering- Characteristics of Filters-Impedance and Lumped element filters-Telephone line filter, Power line filter design, Filter installation and Evaluation,

WEEK 8

Grounding- Measurement of Ground resistance-system grounding for EMI/EMC-Cable shielded grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control. EMI gaskets

WEEK 9 &10 PREMODEL

UNIT IV EMC DESIGN OF PCBS

EMI Suppression Cables-Absorptive, ribbon cables-Devices-Transient protection hybrid circuits

WEEK 11

Component selection and mounting; PCB trace impedance; Routing; Cross talk control, Electromagnetic Pulse-Noise from relays and switches,

WEEK 12

Power distribution decoupling; Zoning;Grounding; VIAs connection; Terminations

UNIT TEST -IV

WEEK 13

UNIT V EMI MEASUREMENTS AND STANDARDS

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors

WEEK 14

EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462. Frequency assignment - spectrum conversation British VDE standards, Euro norms standards in japan - comparisons. EN Emission and Susceptibility standards and Specifications

WEEK- 15 MODEL EXAM

WEEK- 16 MODEL EXAM

WEEK- 17 MODEL EXAM

REFERENCES:

1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, New York, 1996.
2. Clayton R.Paul,” Introduction to Electromagnetic Compatibility”, John Wiley Publications, 2008
3. Henry W.Ott., ”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
4. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Don R.J. White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988.

AP7010 DATA CONVERTERS

WEEK 1

UNIT I SAMPLE AND HOLD CIRCUITS

Sampling switches, Conventional open loop and closed loop sample and hold architecture

WEEK 2

Open loop architecture with miller compensation, multiplexed input architectures

WEEK 3

recycling architecture switched capacitor architecture.

WEEK 4 UNIT TEST -I

UNIT II

SWITCHED CAPACITOR CIRCUITS AND COMPARATORS

Switched-capacitor amplifiers, switched capacitor integrator

WEEK 5

switched capacitor common mode feedback

WEEK 6

Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT TEST -II

WEEK 7

UNIT III DIGITAL TO ANALOG CONVERS

Performance metrics, reference multiplication and division, switching and logic functions in DAC

WEEK 8

Resistor ladder DAC architecture, current steering DAC architecture

WEEK 9& 10 PREMODEL EXAM

UNIT IV ANALOG TO DIGITAL CONVERSION

Performance metric, flash architecture

WEEK 11

Pipelined Architecture, Successive approximation architecture

WEEK 12

Time interleaved architecture

UNIT TEST -IV

WEEK 13

UNIT V PRECISION TECHNIQUES

Comparator offset cancellation, Op Amp offset cancellation

WEEK 14

Calibration techniques Range overlap and digital correction

WEEK- 15 MODEL EXAM

WEEK- 16 MODEL EXAM

WEEK- 17 MODEL EXAM

REFERENCE:

1. Behzad Razavi, “Principles of data conversion system design”, S. Chand and company Ltd, 2000.

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