VELTECH MULTI TECH Dr. RANGARAJAN Dr.SAKUNTHALA ENGINEERING COLLEGE
Accredited by NBA, New Delhi
An ISO 9001:2000 Certified Institution
(Owned by Vel Trust 1997)
Approved by AICTE , New Delhi & Govt. of Tamilnadu & Affiliated to Anna University

SYLLABUS

WEEKLY SCHEDULE

SEMESTER II 2015-16

DEPARTMENT OF ECE
M.E-VLSI DESIGN

2 YEAR COURSE

60, Avadi-Alamathi Road,Chennai-600 062.
Phone:2684106
E-mail:vel multimedia@rediffmail.com
Website : www.vel-tech.org

WEEK DETAILS
YEAR 2016

SL.NO.	WEEK	FROM	TO
1	**WEEK1**	18.01.16	23.01.16
2	**WEEK2**	25.01.16	30.01.16
3	**WEEK3**	01.02.16	06.02.16
4	**WEEK4**	08.02.16	13.02.16
5	**WEEK5**	15.02.16	20.02.16
6	**WEEK6**	22.02.16	27.02.16
7	**WEEK7**	29.02.16	05.03.16
8	**WEEK8**	07.03.16	12.03.16
9	**WEEK9**	16.03.16	20.03.16
10	**WEEK10**	22.03.16	26.03.16
11	**WEEK11**	27.03.16	02.04.16
12	**WEEK12**	03.04.16	09.04.16
13	**WEEK13**	11.04.16	16.04.16
14	**WEEK14**	18.04.16	23.04.16
15	**WEEK15**	25.04.16	30.04.16

THEORY

S.NO	SUBJECT CODE	NAME OF THE SUBJECT
1.	AP7201	Analysis and Design of Analog Integrated Circuits
2.	VL7201	CAD for VLSI Circuits
3.	VL7202	Low Power VLSI Design
4.	VL7005	Physical Design of VLSI Circuits
5.	VL7008	Design of Semiconductor Memories
6.	AP7016	System on Chip Design
PRACTICAL		
7.	VL7211	VLSI DESIGN LAB-II

TEST / EXAM SCHEDULE

SL. NO	SUBJECT CODE	SUBJECT NAME	UNIT TEST I	UNIT TEST II	PRE MODEL EXAM	MODEL EXAM
1	AP7201	Analysis and Design of Analog Integrated Circuits	01.02.16	15.02.16	29.02.06	01.04.16
2	VL7201	CAD for VLSI Circuits	02.02.16	16.02.16	01.03.16	04.04.16
3	VL7202	Low Power VLSI Design	03.02.16	17.02.16	02.03.16	06.04.16
4	VL7005	Physical Design of VLSI Circuits	04.02.16	18.02.16	03.03.16	08.04.16
5	VL7008	Design of Semiconductor Memories	05.02.16	19.02.16	04.03.16	11.04.16
6	AP7016	System on Chip Design	06.02.15	20.02.16	05.03.16	13.04.16

AP7201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

OBJECTIVES:

- To design the single stage amplifiers using pmos and nmos driver circuits with different loads.
- To analyse high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
- To study the different types of current mirrors and to know the concepts of voltage and current reference circuits.

UNIT I SINGLE STAGE AMPLIFIERS

WEEK -1: Common source stage, Source follower, Common gate stage, ,

WEEK-2 :Cascode stage Single ended and differential operation,

WEEK-3: Basic differential pair, Differential pair with MOS loads

UNIT II FREQUENCY RESPONSE AND NOISE ANALYSIS

WEEK-4: Miller effect, Association of poles with nodes, frequency response of common source stage.

WEEK-5 Source followers, Common gate stage, Cascode stage, Differential pair, Statistical
Characteristics of noise,

WEEK-6 Noise in single stage amplifiers, noise in differential amplifiers

WEEK -6: CYCLE TEST-1

UNIT III OPERATIONAL AMPLIFIERS

WEEK -7 : Concept of negative feedback, Effect of loading in feedback networks,

WEEK -8 : Operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps

WEEK -9 Input range limitations Gain boosting, slew rate,
power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION

WEEK - 10: General considerations, Multipole systems, Phase Margin,

WEEK -11 : Compensation of two stage Op Amps,

WEEK -12 : Frequency Compensation,Slewing in two stage Op Amps, Other compensation
techniques.

WEEK -13 :CYCLE TEST-2

UNIT V BIASING CIRCUITS

9

WEEK -14 Basic current mirrors, cascode current mirrors, active current mirrors,

WEEK -15 Voltage references,supply independent biasing,

WEEK -16 Temperature independent references, PTAT current generation,Constant-Gm Biasing.

WEEK -17: MODEL EXAM

REFERENCES:

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design
of Analog Integrated Circuits, 5th Edition, Wiley, 2009.

2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill,
2001

3. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.

4. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley &
sons,Inc., 2003.

5. Phillip E.Allen, DouglasR.Holberg, "CMOS Analog Circuit Design", Second edition,
Oxford University Press, 2002

VL7201 CAD FOR VLSI CIRCUITS

OBJECTIVES:

- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.

 To use the simulation techniques at various levels in VLSI design flow,
 To understand the concepts of various algorithms used for floor planning and routing
techniques.

UNIT I VLSI DESIGN METHODOLOGIES

WEEK -1 Introduction to VLSI Design methodologies - Review of Data structures and algorithms -

WEEK -2 Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational

WEEK -3 Complexity - Tractable and Intractable problems - general purpose methods for
combinatorial optimization.

UNIT II DESIGN RULES

WEEK -4 Layout Compaction - Design rules - problem formulation

WEEK -5 algorithms for constraint graph compaction - placement and partitioning –

WEEK -6 Circuit representation – Placement algorithms – partitioning

WEEK -6 : CYCLE TEST-1

UNIT III FLOOR PLANNING

WEEK -7 Floor planning concepts - shape functions and floorplan sizing

WEEK -8 Types of local routing problems

WEEK -9 Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION

WEEK -10 Simulation - Gate-level modeling and simulation

WEEK -11 Switch-level modeling and simulation

WEEK -12 Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic
Synthesis.

WEEK -13 :CYCLE TEST-2

UNIT V MODELLING AND SYNTHESIS

WEEK -14 High level Synthesis - Hardware models - Internal representation

WEEK -15 Allocation -assignment and scheduling - Simple scheduling algorithm

WEEK -16 - Assignment problem – High level transformations.

WEEK -17 : MODEL EXAM

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic
Publishers, 2002.
3. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”,
World scientific 1999.
4. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing 1987.

VL7202 LOW POWER VLSI DESIGN

OBJECTIVES:

- To know the sources of power consumption in cmos circuits
- To understand the various power reduction techniques and the power estimation
methods.
- To study the design concepts of low power circuits.

UNIT I POWER DISSIPATION

WEEK -1 Hierarchy of limits of power – Sources of power consumption

WEEK -2 Physics of power dissipation in CMOS FET devices

WEEK -3 Basic principle of low power design.

UNIT II POWER OPTIMIZATION

WEEK -4 Logic level power optimization

WEEK -5 Circuit level low power design

WEEK -6 circuit techniques for reducing power consumption in adders and multipliers.

WEEK -6 : CYCLE TEST-1

UNIT III DESIGN OF LOW POWER CIRCUITS

WEEK -7 Computer arithmetic techniques for low power system

WEEK -8 rreducing power consumption in memories – low power clock,

WEEK -9 Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION

WEEK -10 Power Estimation technique – logic power estimation

WEEK -11 Simulation power analysis

WEEK -12 Probabilistic power analysis.

WEEK -13 :CYCLE TEST-2

UNIT V SYNTHESIS AND SOFTWARE DESIGN

WEEK -13 Synthesis for low power

WEEK -14 Behavioral level transform

WEEK -15 software design for low power.

WEEK -17 : MODEL EXAM

REFERENCES:

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.

2. Dimitrios Soudris, Christians Pignet, Costas Goutis, "Designing CMOS Circuits for Low
Power", Kluwer, 2002.

3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.

4.A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”,
Kluwer,1995.
5. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John
Wiley and sons, inc. 2001.
8. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing.

VL7005 PHYSICAL DESIGN OF VLSI CIRCUITS

OBJECTIVE:

To introduce the physical design concepts such as routing, placement, partitioning and
packaging and to study the performance of circuits layout designs, compaction techniques.

UNIT I INTRODUCTION TO VLSI TECHNOLOGY

WEEK -1 Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining

WEEK -2 Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea
of gates,field programmable gate array(FPGA)-layout methodologies

WEEK -3 Packaging-Computational Complexity-Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH

WEEK -4 Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin HeuristicRatiocutpartitionwith capacity and i/o constrants.

WEEK -5 Floor planning: Rectangular dual floor planninghierarchialapproach- simulated annealing Floor plan sizingPlacement: Cost function- force directed method- placement by simulated annealingpartitioning

WEEK -6 placement- module placement on a resistive network – regular placementlinear placement.

WEEK -6 : CYCLE TEST-1

UNIT III ROUTING USING TOP DOWN APPROACH

WEEK -7 Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential
Approaches- hierarchial approaches- multicommodity flow based techniques- Randomised

WEEK -8 Routing- One Step approach- Integer Linear Programming Detailed Routing: Channel

WEEK -9 Routing- Switch box routing.Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT

WEEK -10 Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees.Timing – Driven Placement

WEEK -11 Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization Click Skew Problem-

WEEK -12 Buffered Clock Trees. Minimization: constrained via Minimizationunconstrained via
Minimization- Other issues in minimization

WEEK -13 :CYCLE TEST-2

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION

WEEK -14 Planar subset problem(PSP)- Single Layer Global Routing-Single Layer detailed Routing-Wire length and bend minimization technique

WEEK -15 Over The Cell (OTC) Routing Multiple chip modules(MCM)-Programmable Logic Arrays

WEEK -16 Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

WEEK -17 : MODEL EXAM

REFERENCES:

1. Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", Mc Graw Hill
International Edition 1995
2. Preas M. Lorenzatti, " Physical Design and Automation of VLSI systems", The Benjamin
Cummins Publishers, 1998.

VL7008 DESIGN OF SEMICONDUCTOR MEMORIES

OBJECTIVES:

1. To study the architectures for SRAM and DRAM
2. To know about various non-volatile memories.
3. To study the fault modelling and testing of memories for fault detection.
4. To learn the radiation hardening process and issues for memory.

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES

WEEK -1 Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM
Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies

WEEK -2 Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and
Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs)

WEEK -3 DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

UNIT II NONVOLATILE MEMORIES

WEEK -4 Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV)

WEEK -5 Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs
WEEK -6 Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-
Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory
Architecture.
WEEK -6 : CYCLE TEST-1

UNIT III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE

WEEK -7 RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM **WEEK -8** Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling
WEEK -9 TestingApplication Specific Memory Testing

UNIT IV RELIABILITY AND RADIATION EFFECTS

WEEK -10 General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for ReliabilityReliability
WEEK -11 Test Structures-Reliability creening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing
WEEK -12 Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.
WEEK -13 :CYCLE TEST-2

UNIT V PACKAGING TECHNOLOGIES

WEEK -14 Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening
TechniquesRadiation Hardening Process and Design Issues-Radiation Hardened Memory
Characteristics-Radiation Hardness Assurance and Testing

WEEK -15 Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto resistive.
WEEK -16 Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.
WEEK -17 : MODEL EXAM
REFERENCES:
1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability
",Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Tegze P.Haraszti, "CMOS Memory Circuits", Kluwer Academic publishers, 2001.
3. Betty Prince, " Emerging Memories: Technologies and Trends", Kluwer Academic

AP7016 SYSTEM ON CHIP DESIGN

OBJECTIVES :
1. To design combinational and sequential logic networks.
2. To learn optimization of power in combinational and sequential logic machines.
3. To study the design principles of FPGA and PLA.
4. To learn various floor planning methods for system design.

UNIT I LOGIC GATES
WEEK -1 Introduction. Combinational Logic Functions. Static Complementary Gates.
WEEK -2 Switch Logic.Alternative Gate Circuits. Low-Power Gates.
WEEK -3 Delay Through Resistive Interconnect. Delay Through Inductive Interconnect. Objectives

UNIT II COMBINATIONAL LOGIC NETWORKS

WEEK -4 Introduction. Standard Cell-Based Layout. Simulation. Combinational Network Delay.

WEEK -5 Logic and interconnect Design. Power Optimization.

WEEK -6 Switch Logic Networks. Combinational Logic Testing.

WEEK -6 : CYCLE TEST-1

UNIT III SEQUENTIAL MACHINES

WEEK -7 Introduction. Latches and Flip-Flops. Sequential Systems and Clocking Disciplines.

WEEK -8 Sequential System Design. Power Optimization.

WEEK -9 Design Validation. Sequential Testing.

UNIT IV SUBSYSTEM DESIGN

WEEK -10 Introduction. Subsystem Design Principles. Combinational Shifters.

WEEK -11 Adders. ALUs.Multipliers. High-Density Memory.

WEEK -12 FieldProgrammable Gate Arrays. Programmable Logic Arrays. References. Problems.

WEEK -13 :CYCLE TEST-2

UNIT V FLOOR-PLANNING

WEEK -14 Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, switchbox Routing,

WEEK -15 Power Distribution, Clock Distributions, Floor-planning Tips,Design Validation.

WEEK -16 Off-Chip Connections – Packages, The I/O Architecture, PAD Design.

WEEK -17 : MODEL EXAM

REFERENCES

1. Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd
Edition , 2008.

2. Wayne Wolf , “ Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition ,

VL7211 VLSI DESIGN LABORATORY II

1. Design and simulate frequency response and noise analysis of any Source followers
2. Design and simulate operational amplifier performance parameters - One-stage Op Amps,

   Two-stage Op Amps
3. Design and simulate cascode current mirrors and active current mirrors
4. Design of various routing - local routing, Area routing, channel routing and global Routing.
5. Design and Simulation of Gate-level modeling
6. Design and Simulation of Switch-level modeling
7. Modeling and synthesis of simple scheduling algorithm
8. Design and implement reducing power consumption in memories
9. Design and simulate Power Estimation.