VEL TECH MULTI TECH
Dr RANGARAJAN Dr.SAKUNTHALA ENGINEERING COLLEGE

(An ISO 9001: 2008 Certified Institution)
(Owned by Vel Trust)
(Approved by Govt. of Tamil Nadu and affiliated to Anna University)

SYLLABUS

WEEKLY SCHEDULE

III SEMESTER 2015 - 2016

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II YEAR DEGREE COURSE

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WEEK DETAILS

SL.NO.	WEEK	FROM	TO
1	**WEEK1**	**24.06.2015**	**26.06.2015**
2	**WEEK2**	**29.06.2015**	**03.07.2015**
3	**WEEK3**	**06.07.2015**	**10.07.2015**
4	**WEEK4**	**13.07.2015**	**17.07.2015**
5	**WEEK5**	**20.07.2015**	**24.07.2015**
6	**WEEK6**	**27.07.2015**	**28.07.2015**
7	**WEEK7**	**03.08.2015**	**07.08.2015**
8	**WEEK8**	**10.08.2015**	**14.08.2015**
9	**WEEK9**	**17.08.2015**	**21.08.2015**
10	**WEEK10**	**24.08.2015**	**28.08.2015**
11	**WEEK11**	**31.08.2015**	**04.09.2015**
12	**WEEK12**	**07.09.2015**	**11.09.2015**
13	**WEEK13**	**14.09.2015**	**18.09.2015**
14	**WEEK14**	**21.09.2015**	**25.09.2015**
15	**WEEK15**	**28.09.2015**	**30.09.2015**
16	**WEEK16**	**05.10.2015**	**09.10.2015**
17	**WEEK17**	**12.10.2015**	**16.10.2015**
18	**WEEK18**	**19.10.2015**	**20.10.2015**
19	**WEEK19**	**27.10.2015**	**30.10.2015**

SUBJECT CONTENTS

SL.NO	SUBJECT CODE	SUBJECT NAME
THEORY		
1	VL7301	TESTING OF VLSI CIRCUITS
2	AP 7301	ELECTROMAGNET IC INTERFERENCE AND
3	AP 7010	DATA CONVERTERS
PRACTICAL		
4	VL7311	PROJECT WORK (PHASE I)

TEST / EXAM SCHEDULE

SL.NO	SUBJECT CODE	SUBJECT NAME	UNIT TEST I	UNIT TEST II	Pre Model Exam	UNIT TEST IV
1	VL7301	Testing of VLSI circuits	13.07.2015	03.08.2015	21.08.2015	14.09.2015
2	AP 7301	Electromagnet IC Interference and Compatibility	14.07.2015	04.08.2015	22.08.2015	15.09.2015
3	AP 7010	Data Converters	15.07.2015	05.08.2015	24.08.2015	16.09.2015

SL.NO	SUBJECT CODE	SUBJECT NAME	MODEL EXAM
1	VL7301	Testing of VLSI circuits	05.10.2015
2	AP 7301	Electromagnet IC Interference and Compatibility	06.10.2015
3	AP7010	Data converters	07.10.2015

VL7301 TESTING OF VLSI CIRCUITS

WEEK 1

UNIT I TESTING AND FAULT MODELLING

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models

WEEK 2

Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation

WEEK 3

Delay models – Gate Level Event – driven simulation.

WEEK 4 UNIT TEST -I

UNIT II TEST GENERATION

Test generation for combinational logic circuits – Testable combinational logic circuit design

WEEK 5

Test generation for sequential circuits

WEEK 6

design of testable sequential circuits.

WEEK 7 UNIT TEST -II

WEEK 8

UNIT III DESIGN FOR TESTABILITY

Design for Testability – Ad-hoc design

WEEK 9

generic scan based design – classical scan based design – system level DFT approaches

WEEK 10 UNIT TEST -III

UNIT IV SELF – TEST AND TEST ALGORITHMS

Built-In self Test – test pattern generation for BIST

WEEK 11 Circular BIST – BIST Architectures – Testable Memory Design

WEEK 12

Test Algorithms – Test generation for Embedded RAMs.

WEEK 13 UNIT TEST -IV

WEEK 14

UNIT V Z - FAULT DIAGNOSIS

Logical Level Diagnosis – Diagnosis by UUT reduction

WEEK 15

Fault Diagnosis for Combinational Circuits – Self-checking design

WEEK-16

System Level Diagnosis.

WEEK- 17 UNIT TEST –V

WEEK- 18 MODEL EXAM

TOTAL: 45 PERIODS

REFERENCES:

1. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable
Design", Jaico Publishing House,2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory
and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice
Hall International, 2002.

AP7301 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

WEEK 1

UNIT I EMI/EMC CONCEPTS

EMI-EMC definitions and Units of parameters; Sources and victim of EMI

WEEK 2

Conducted and Radiated EMI Emission and Susceptibility;

WEEK 3

Transient EMI, ESD; Radiation Hazards

WEEK 4 UNIT TEST -I

UNIT II EMI COUPLING PRINCIPLES

Conducted, radiated and transient coupling; Common ground impedance coupling

WEEK 5

Common mode and ground loop coupling ; Differential mode coupling; Near field cable to cable coupling, cross talk

WEEK 6

Field to cable coupling ; Power mains and Power supply coupling.

WEEK 7 UNIT TEST -II

WEEK 8

UNIT III EMI CONTROL TECHNIQUES

Shielding- Shielding Material-Shielding integrity at discontinuties, Filtering- Characteristics of

Filters-Impedance and Lumped element filters-Telephone line filter, Power line filter design, Filter

installation and Evaluation,

WEEK 9

Grounding- Measurement of Ground resistance-system grounding for

EMI/EMC-Cable shielded grounding, Bonding, Isolation transformer, Transient suppressors, Cable

routing, Signal control. EMI gaskets

WEEK 10 UNIT TEST -III

UNIT IV EMC DESIGN OF PCBS

EMI Suppression Cables-Absorptive, ribbon cables-Devices-Transient protection hybrid circuits

WEEK 11

Component selection and mounting; PCB trace impedance; Routing; Cross talk contro

WEEK 12

Electromagnetic Pulse-Noise from relays and switches, Power distribution decoupling; Zoning;

Grounding; VIAs connection; Terminations

WEEK 13 UNIT TEST -IV

WEEK 14

UNIT V EMI MEASUREMENTS AND STANDARDS

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic

chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors

WEEK 15

EMI Rx and

spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

Frequency assignment - spectrum conversation

WEEK-16

British VDE standards, Euro norms standards in japan - comparisons. EN Emission and Susceptibility standards and Specifications

WEEK- 17 UNIT TEST –V

WEEK- 18 MODEL EXAM

REFERENCES:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, New York, 1996.
2. Clayton R.Paul," Introduction to Electromagnetic Compatibility", John Wiley Publications, 2008
3. Henry W.Ott., "Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
4. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Don R.J. White Consultant Incorporate, "Handbook of EMI/EMC" , Vol I-V, 1988.

AP7010 DATA CONVERTERS

WEEK 1

UNIT I SAMPLE AND HOLD CIRCUITS

Sampling switches, Conventional open loop and closed loop sample and hold architecture

WEEK 2

Open loop architecture with miller compensation, multiplexed input architectures

WEEK 3

recycling architecture switched capacitor architecture.

WEEK 4 UNIT TEST -I

UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS

WEEK 5

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback

WEEK 6

Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

WEEK 7 UNIT TEST -II

WEEK 8

UNIT III DIGITAL TO ANALOG CONVERS

Performance metrics, reference multiplication and division, switching and logic functions in DAC

WEEK 9

Resistor ladder DAC architecture, current steering DAC architecture

WEEK 10

UNIT IV ANALOG TO DIGITAL CONVERSION

Performance metric, flash architecture

WEEK 11

Pipelined Architecture, Successive approximation architecture

WEEK 12

Time interleaved architecture

WEEK 13 UNIT TEST -IV

WEEK 14

UNIT V PRECISION TECHNIQUES

Comparator offset cancellation, Op Amp offset cancellation

WEEK 15

Calibration techniques

WEEK-16

Range overlap and digital correction

WEEK- 17 UNIT TEST –V

WEEK- 18 MODEL EXAM

REFERENCE:

1. Behzad Razavi, “Principles of data conversion system design”, S. Chand and company Ltd, 2000.

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